# A Holding Voltage Adjustment Technique of SCR for ESD Protection

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**Abstract:** Optimizing the holding voltage of SCR to avoid the latch-up risk has been focused on by researchers recent years. A holding voltage adjustment technique of SCR is presented and discussed in this paper, with the devices implemented in a 0.6μm SOI process. Based on the holding voltage calculation, an external resistor is paralleled with the parasitic $P_{tub}$ resistor to reduce the effective resistance to keep the holding state, leading to higher holding voltage. The proposed SCR (PSCR) is investigated with Transmission Line Pulse generator (TLP). The characterization results show that the holding voltage of the proposed structure can be elevated by the paralleled external resistor $R_e$, and the lower resistance of $R_e$, the higher holding voltage can be achieved. Meanwhile, the connection methods of $R_e$ are investigated with different emitter ratios of $Q_{NPN}$, indicating the trade-off between the holding voltage and failure current.

## 1. Introduction

ESD (Electrostatic discharge) became a problem in the electronics industry since the late of 1970s. The ESD events caused by human body resulted massive device failures and yield losses. With the recognition of the circumstances, the ESD protection design with device, circuit and process optimizations were improved to enhance the robustness of the electronic products. Among the protection devices, SCR is applied widely for strong snapback, efficient shunt capability and small area. However, latch up risk is inevitable for traditional SCR device aimed for on-chip ESD protection. Increasing the holding voltage above the power supply rail or signal range can avoid the danger. Adding several diodes to the SCR [1] and stacking the SCRs or other devices [2] are solutions to increase the SCR's holding voltage. The improved holding voltage is the summation of the individual devices. Some researches to modulate the current path condition to elevate the holding voltage based on the principle of intrinsic SCR. Increasing the base width of the parasitic bipolar junction transistor [3] can lengthen the current path to increase the voltage drop between the terminals. Huang and Ker introduced additional parasitic PNP BJT to partially shunt the positive feedback current to realize higher holding voltage [4]. The segmented technique proposed and improved by [5][6] to reduce the emitter efficiency of parasitic transistors, and achieving higher

holding voltage without extra silicon cost. An interesting method is proposed in [7], using the paralleled external resistor to optimize the conducting resistance to adjust the holding voltage. Based on the previous researches and the layout arrangement, a holding voltage adjustment technique of SCR for ESD protection is investigated in this paper.

## 2. Holding Voltage Analysis of the SCR

The layout and sectional view of the traditional SCR are shown in Fig. 1 (a). The P+ diffusion in the NW plays the role of the anode where holes are injected into the NW, connected to the N+ tap of NW to form the positive feedback loop. The N+ in Ptub and P+ taps are shorted as the cathode of SCR. To analyze the holding voltage of the SCR, the equivalent schematic composed with first order parasitic components is illustrated in Fig. 1 (b). The $Q_{PNP}$ and $Q_{NPN}$ denote the bipolar transistors formed by P+ in NW-NW-Ptub and NW-Ptub-N+ in Ptub, respectively. The RNW and RPtub are the equivalent resistance of NW and Ptub. The Rs1 and Rs2 are the parasitic resistors along the conducting path. According to [7]-[9], the holding voltage of SCR can be expressed as,

$$V_H = V_{CEP} + V_{BEN} \times \left[ 1 + \frac{R_{s2}}{R_{Ptub} // R_e} \right] \tag{1}$$

where the $V_{CEP}$ and $V_{BEN}$ are the collector-emitter voltage drop of $Q_{PNP}$ and the base-emitter voltage drop of $Q_{NPN}$. To increase the holding voltage, the $R_{Ptub}$ can be reduced by paralleled with an external resistor.

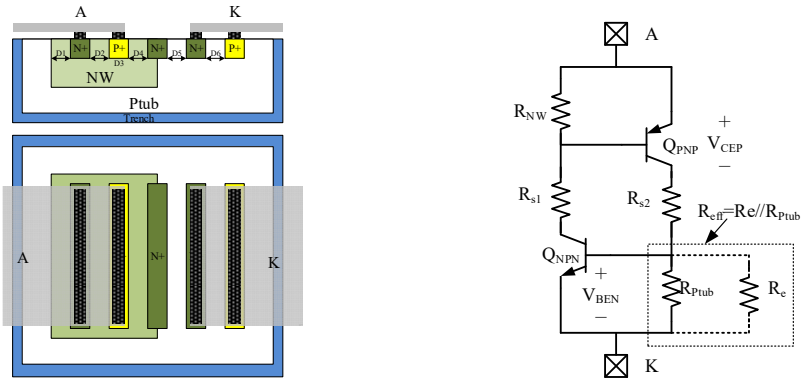



Figure 1 The traditional SCR: (a) layout and sectional view, (b) equivalent schematic

The next section focuses on a complementation of the proposed SCR device to evaluate the holding voltage adjustment technique.

## 3. Principles of the Proposed SCR

The external resistor can be embedded with many methods. It's well known for us that the MOSFET can be used as the resistor with specific bias voltage [7]. The segmented diffusion regions connect to the resistor directly [10]-[11], but the connection ratio of the diffusion areas are not discussed. The proposed layout sketches called PSCR is shown in Figure 2.

The external resistor is realized with poly layer, and connected between the base of the $Q_{NPN}$ and the cathode of the PSCR. The P+ taps are interweave with the N+ diffusion regions in $P_{tub}$ for uniform of the current distribution, since the current on $R_e$ is the total enormous ESD shunt current. Obviously, interweaved ratio can be changed according to the current capability and performance of the device.

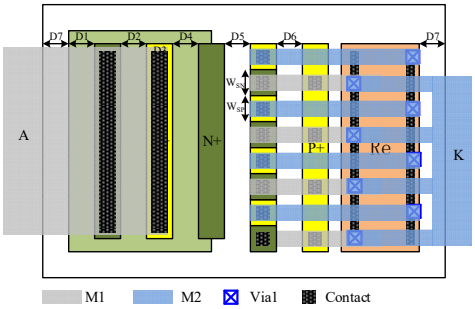
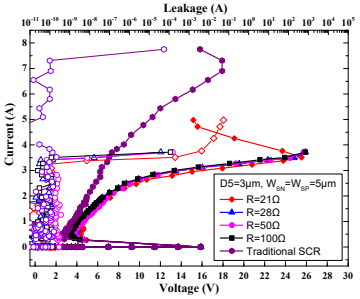



Figure 2 The proposed SCR (PSCR) layout sketch

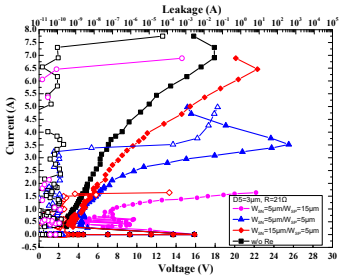
## 4. Measurement Results Comparison and Discussion

With the resistor paralleled calculation equation, the total resistance always is smaller than the individual ones. Regardless of the resistance of Re, it's predicted that the holding voltage will be higher than the traditional SCR. The ESD protection characteristics of the traditional and proposed devices with different layout parameters are investigated using TLP pulses with a 10 ns rise time and 100 ns pulse width. The TLP characteristics of the PSCR with different $R_e$ are measured and compared in Figure 3. The resistance of $R_e$ consists of the resistances of poly strip and contacts. All the devices under test hold the dimensions except the different $R_e$ value. The holding voltage increases from 3.08V to 4.24V with different $R_e$ of 21Ω, 28Ω, 50Ω and 100Ω, while the holding voltage of the traditional SCR illustrated in Figure 1 is only 2.54V. With the $R_e$ increasing, the $R_{eff}$ is determined by the intrinsic $R_{Ptub}$, leading to the holding voltage PSCR reaching that of the traditional SCR. However, the failure current of the proposed SCR with $R_e$ is only about half of that of the traditional counterpart ($I_{t2}$, ~3.5A to ~7.3A), since the segmentation layout for $R_e$ connection reduced the emitter area of the $Q_{NPN}$.




| | R | $V_{t1}$(V) | $V_H$(V) | $I_{t2}$(A) |
|---|---|---|---|---|
| Traditional | — | 15.88 | 2.54 | 7.31 |
| PSCR_1 | 21 | 15.86 | 4.24 | 3.39 |
| PSCR_2 | 28 | 15.89 | 3.19 | 3.5 |
| PSCR_3 | 50 | 15.86 | 3.21 | 3.41 |
| PSCR_4 | 100 | 15.86 | 3.08 | 3.51 |

Figure 3 The TLP characteristics of traditional and PSCR with $R_e$ of 21Ω, 28Ω, 50Ω and 100Ω




| | $W_{SN}$(μm) | $W_{SP}$(μm) | $V_{t1}$(V) | $V_H$(V) | $I_{t2}$(A) |
|---|---|---|---|---|---|
| Traditional SCR | — | — | 15.88 | 2.54 | 7.31 |
| PSCR_1 | 5 | 5 | 15.86 | 4.24 | 3.39 |
| PSCR_5 | 15 | 5 | 15.9 | 2.99 | 6.46 |
| PSCR_6 | 5 | 15 | 15.86 | 4.65 | 1.59 |

Figure 4 The TLP characteristics of traditional and PSCR with different emitter ratio of the $Q_{NPN}$ ($R_e$=21Ω, D5=3μm)

For the PSCR with different emitter ratio of the $Q_{NPN}$, the holding voltage increases with the reduction of the N+ diffusion area. It must be noted that the failure current decreases rapidly with the ratio of N+ diffusion. When the $W_{SN}$=5μm and $W_{SP}$=15μm, the highest $V_H$ of 4.65V and the lowest $I_{t2}$ of 1.59A are resulted corresponding with the theory predictions. Obviously, the trade-off between the $V_H$ and $I_{t2}$ has to be considered. The contacting area of P+ tap in $P_{tub}$ and external resistor $R_e$ isn't related with the failure current level directly.

## 5. Conclusion

A holding voltage adjustment technique of SCR with external resistor is discussed and investigated with a serial of devices implemented in a 0.6μm SOI process in this paper. The lower external resistance, the higher holding voltage can be achieved according to the theory calculation. The TLP characterization results show that the holding voltage of the proposed structures can be elevated by the paralleled external resistor $R_e$. The experiment results are consistent with the theory analysis, demonstrating that the technique is available to adjust the holding voltage of SCR for ESD protection.

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